FIG.1

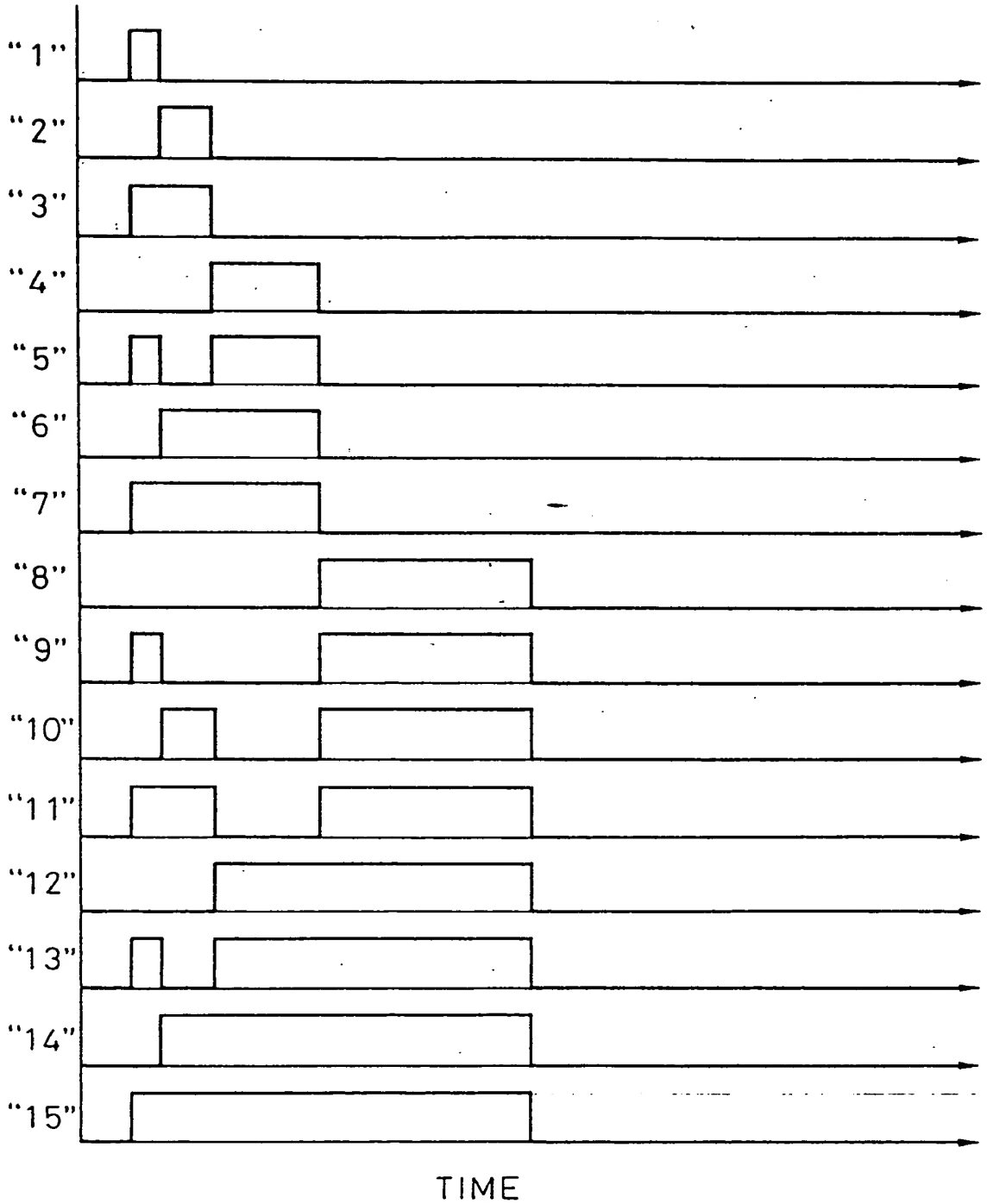
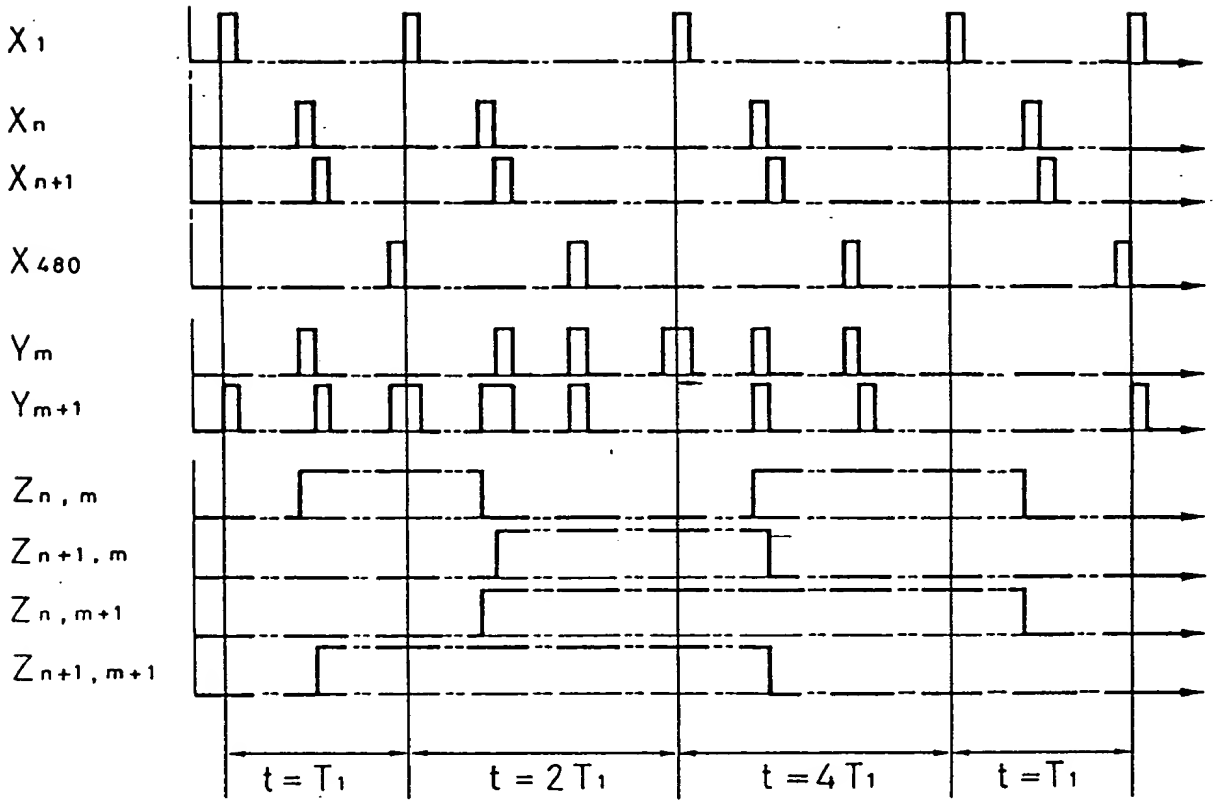


FIG. 2



$Z_{n,m}$: $T_1 + 4T_1 = 5T_1$ ⟶ "5"
$Z_{n+1,m}$: $2T_1$ ⟶ "2"
$Z_{n,m+1}$: $2T_1 + 4T_1 = 6T_1$ ⟶ "6"
$Z_{n+1,m+1}$: $T_1 + 2T_1 = 3T_1$ ⟶ "3"

FIG. 3

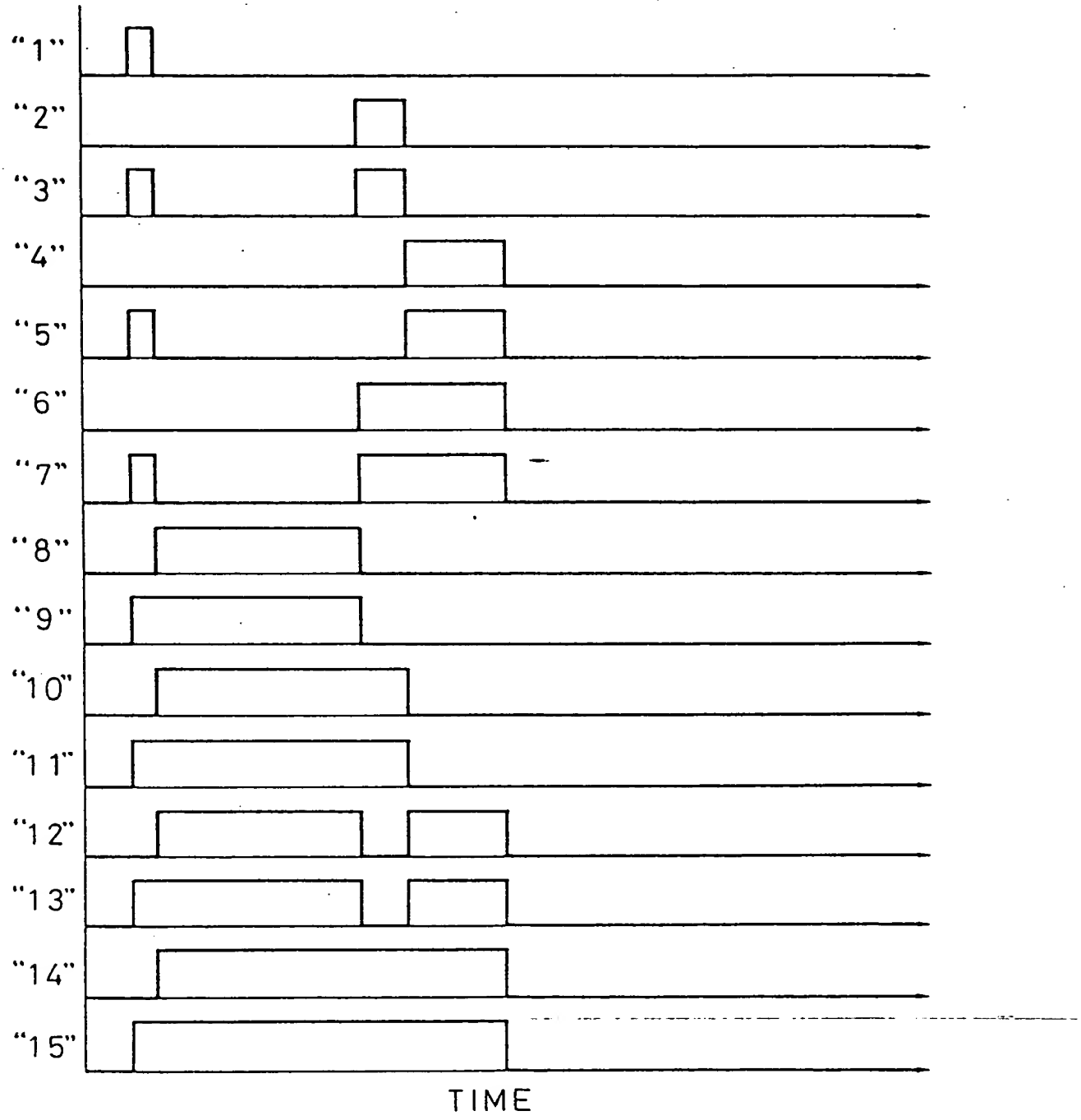
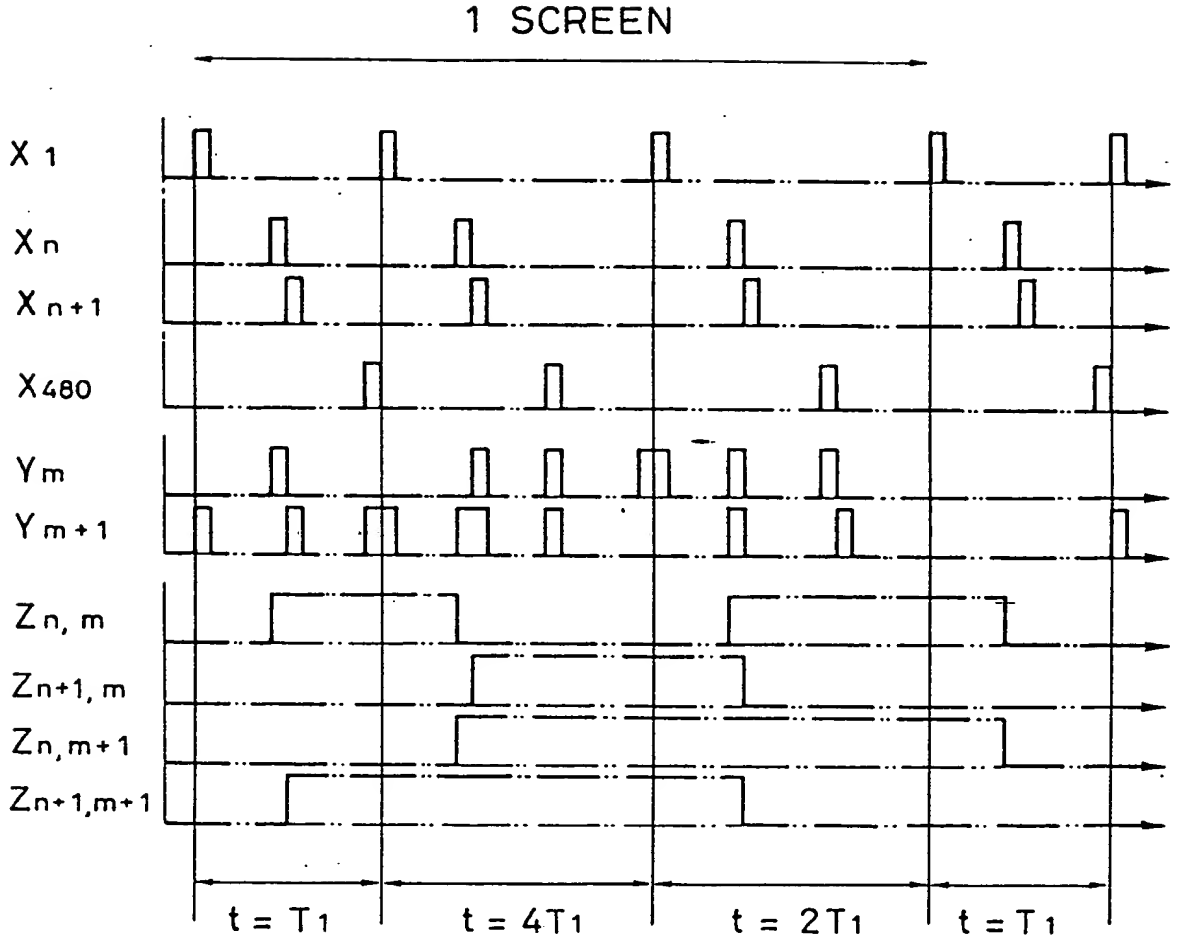


FIG. 4



$Z_{n,m}$: $T_1 + 2T_1 = 3T_1$ → "3"

$Z_{n+1,m}$: $4T_1$ → "4"

$Z_{n,m+1}$: $4T_1 + 2T_1 = 6T_1$ → "6"

$Z_{n+1,m+1}$: $T_1 + 4T_1 = 5T_1$ → "5"

FIG. 5

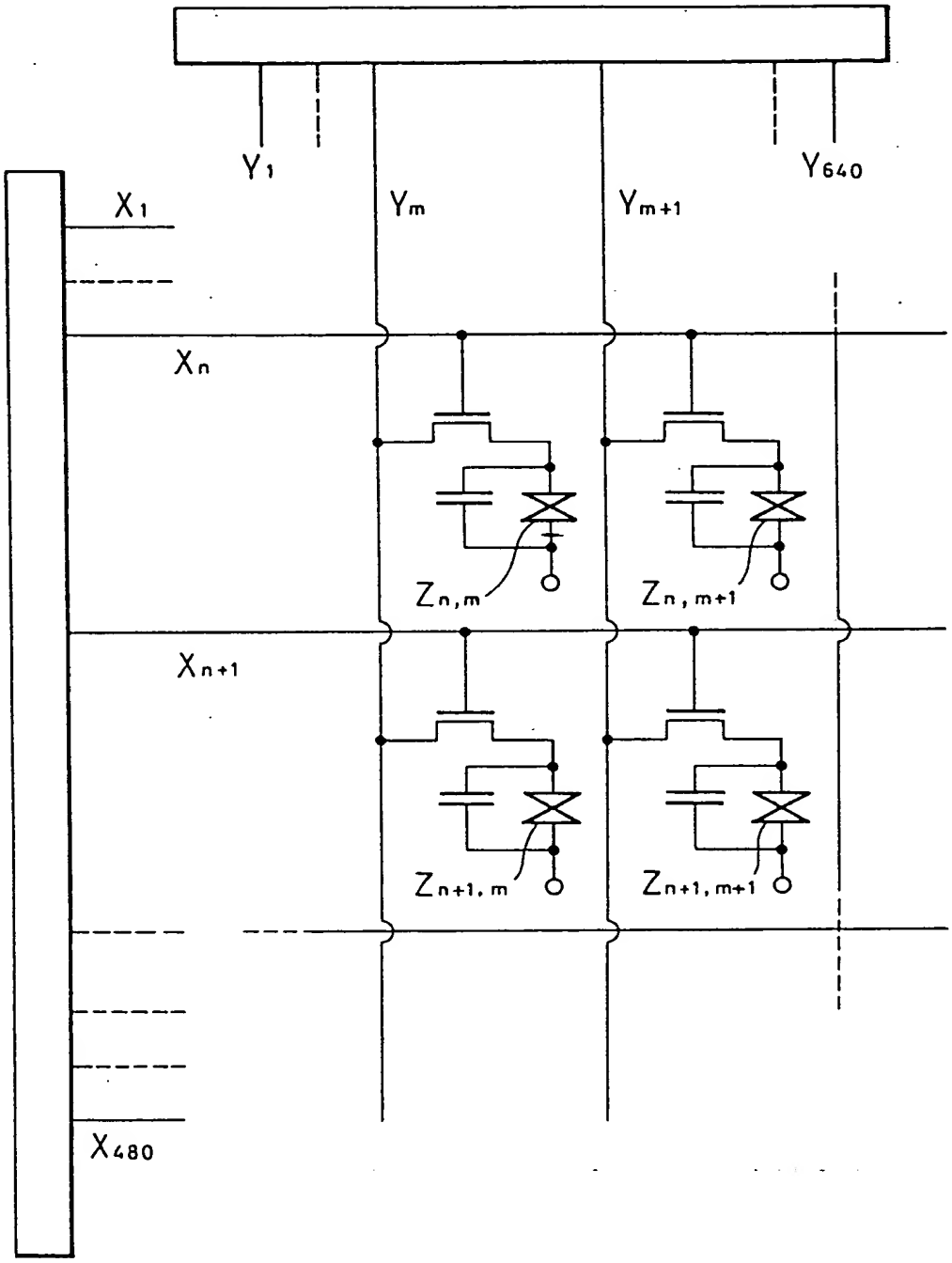


FIG.6

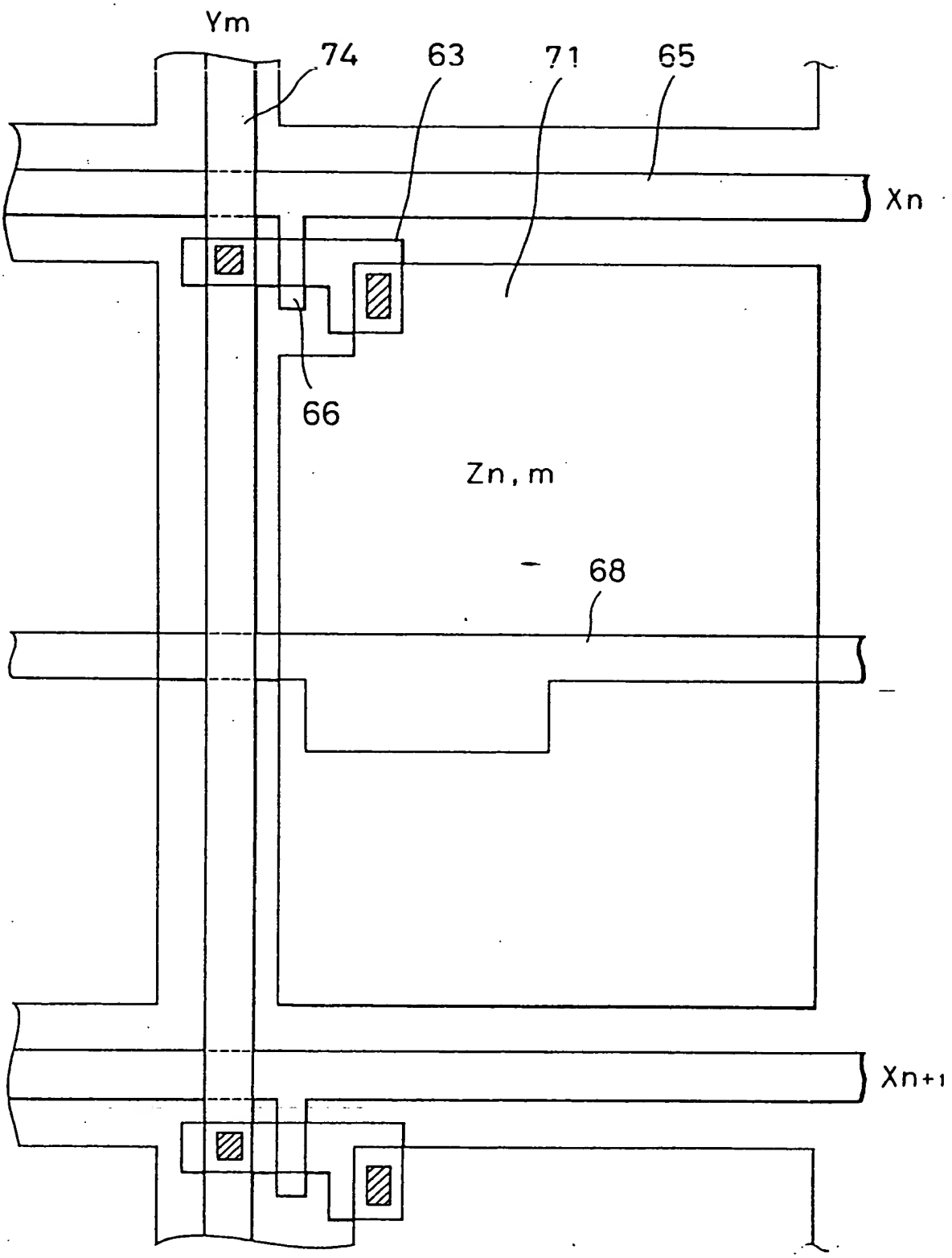


FIG. 7(A)

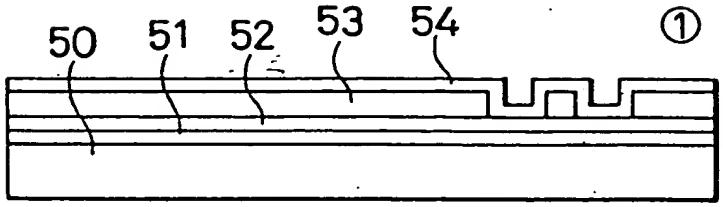


FIG. 7(B)

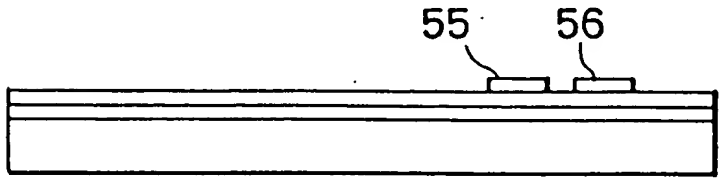


FIG. 7(C)

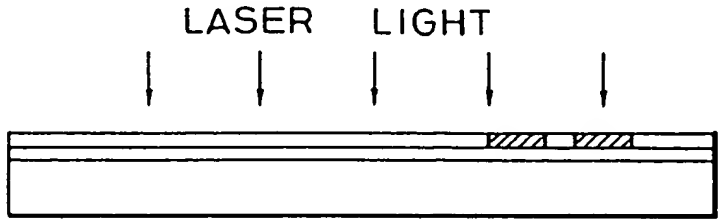


FIG. 7(D)

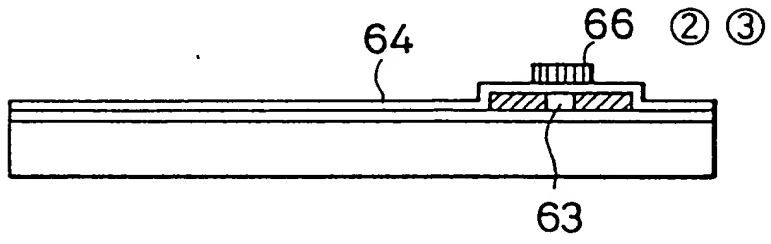


FIG. 7(E)

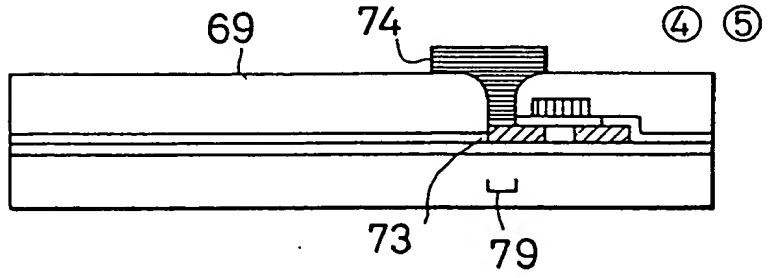
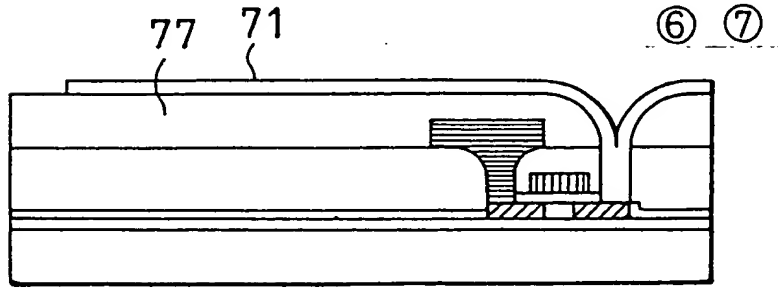


FIG. 7(F)



0095408 '96 8 04 5 60

FIG. 8(A)

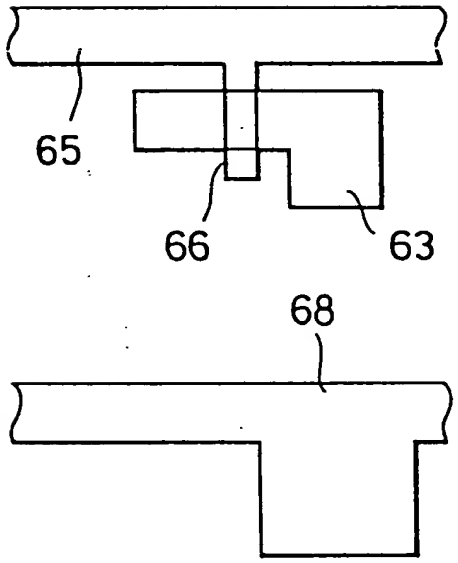


FIG. 8(B)

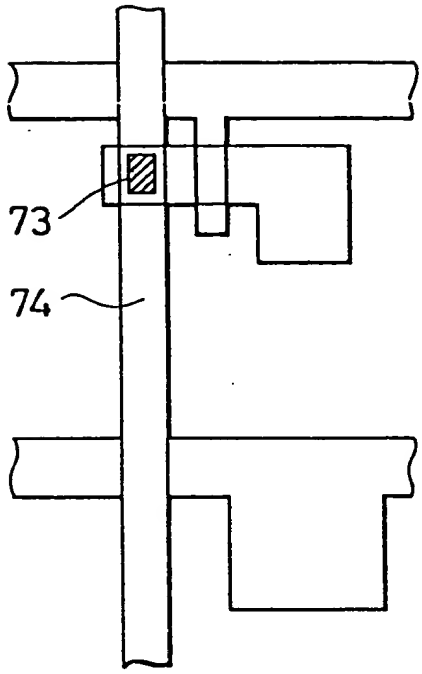


FIG. 8(C)

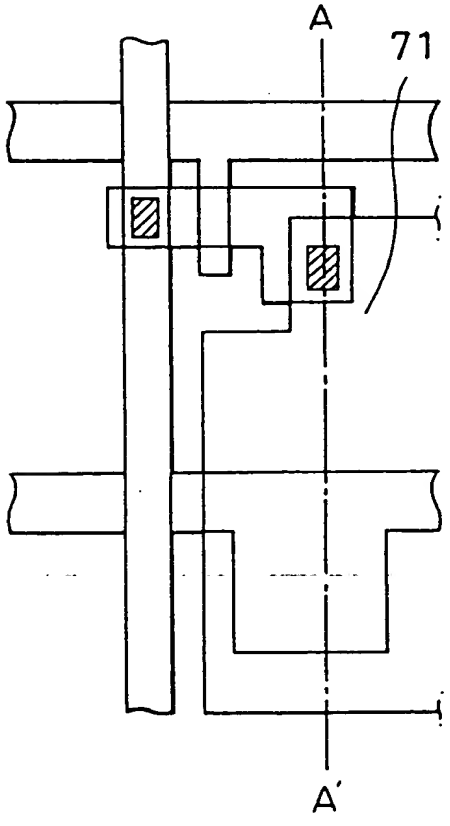
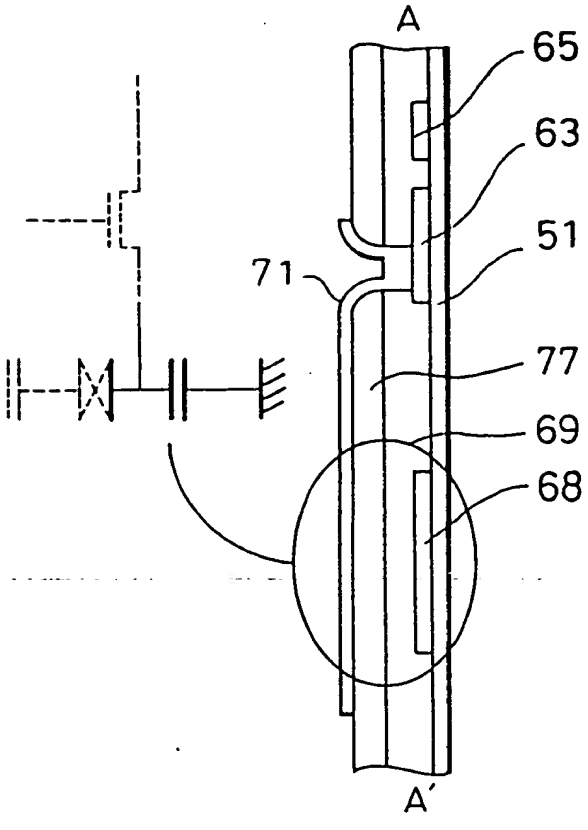


FIG. 8(D)



0095408 '96 8 26

FIG. 9(A)

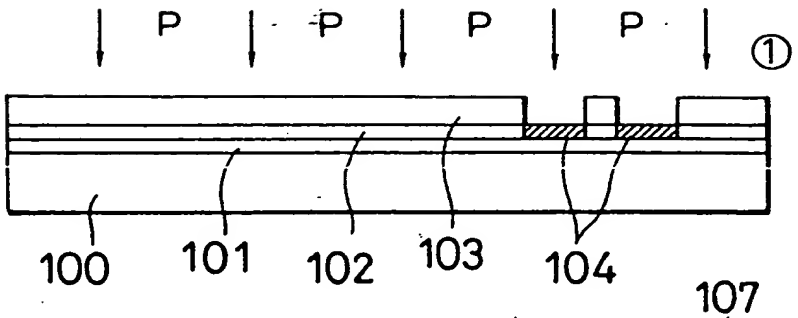


FIG. 9(B)

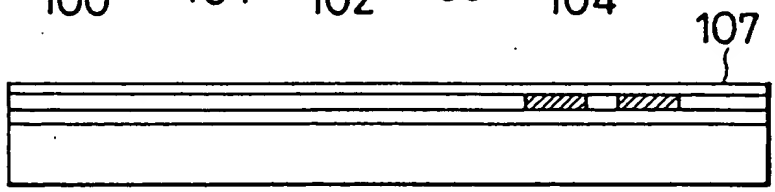


FIG. 9(C)

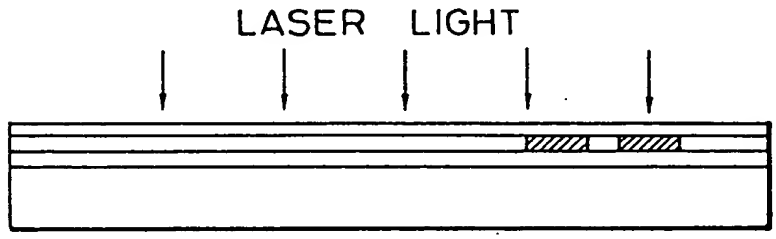


FIG. 9(D)

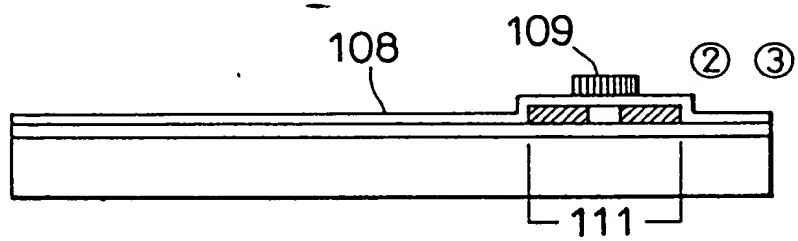


FIG. 9(E)

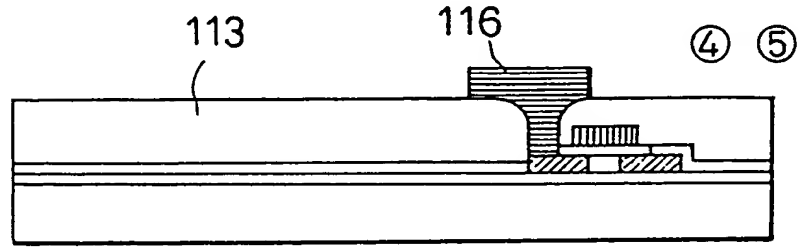


FIG. 9(F)

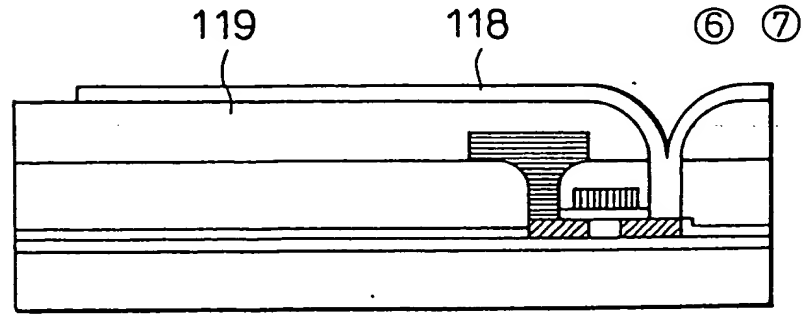


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FIG. 10 (A)

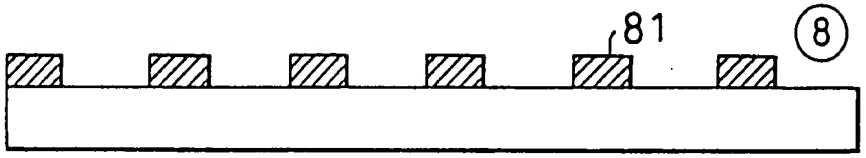


FIG. 10 (B)

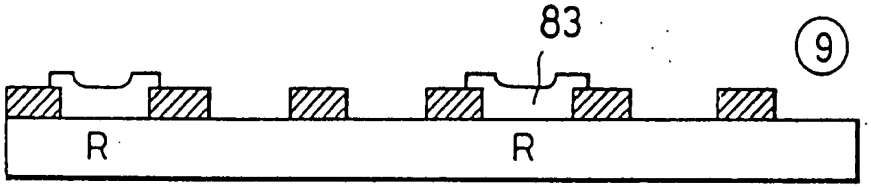


FIG. 10 (C)

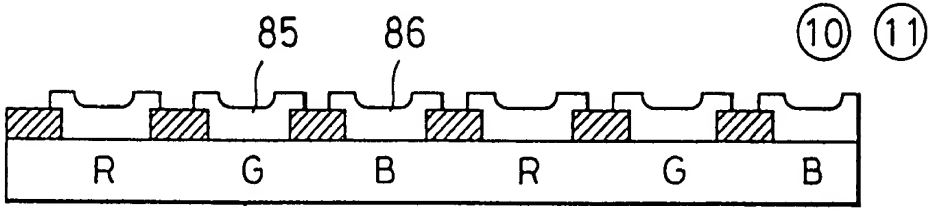


FIG. 10(D)

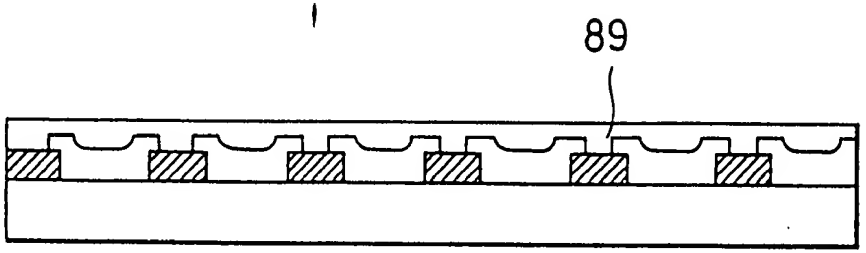


FIG. 10(E)

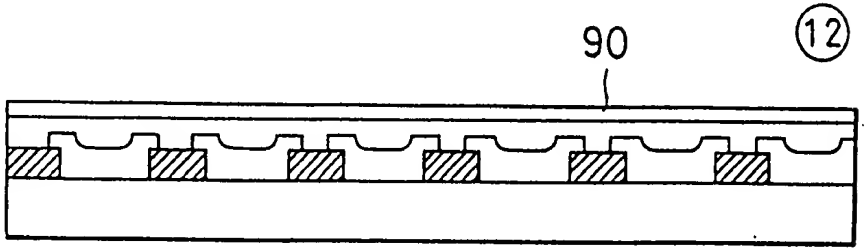


FIG. 1 1

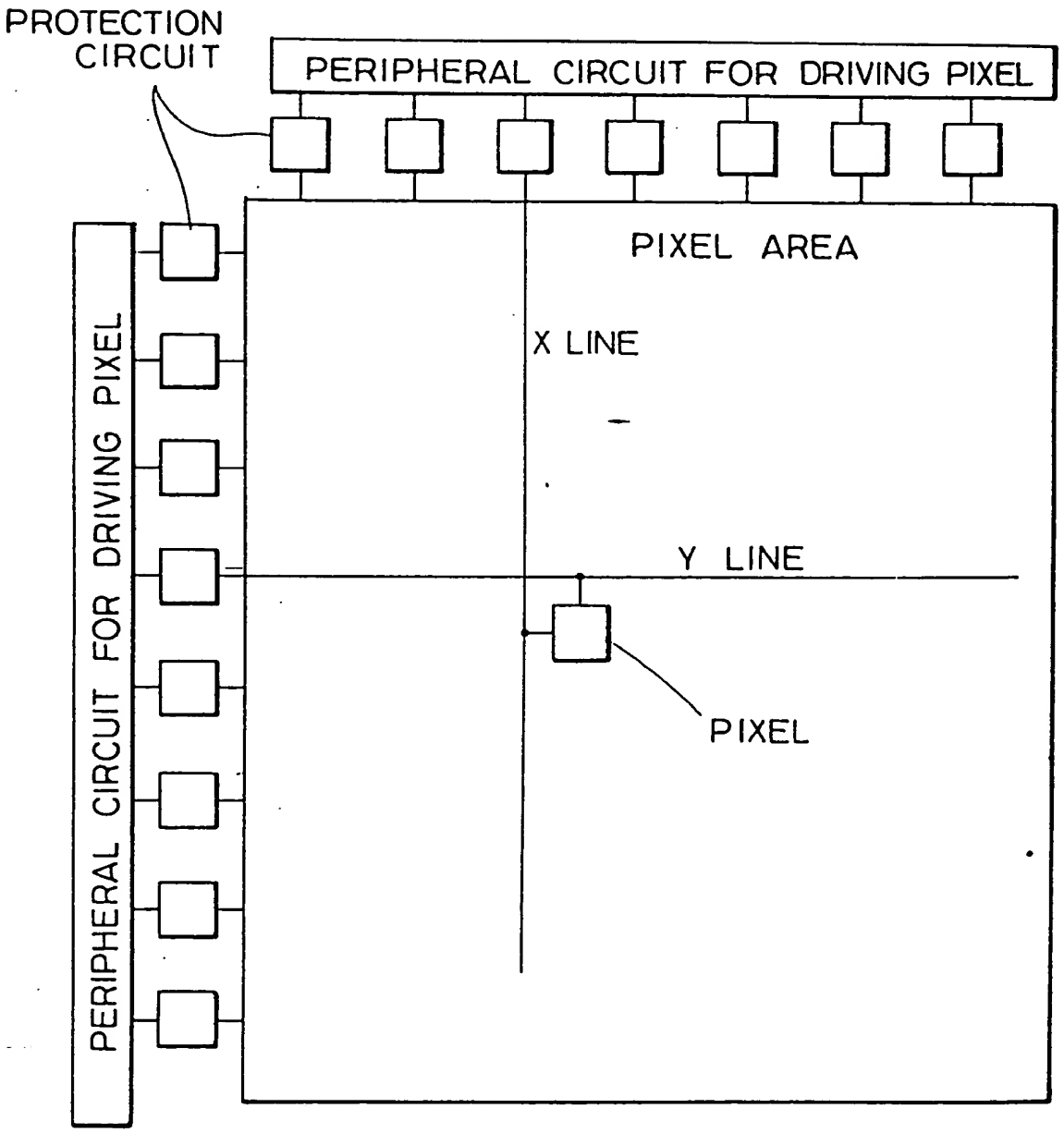

PROTECTION CIRCUIT
PERIPHERAL CIRCUIT FOR DRIVING PIXEL
PIXEL AREA
X LINE
Y LINE
PIXEL
PERIPHERAL CIRCUIT FOR DRIVING PIXEL

FIG.12(A) FIG.12(B)

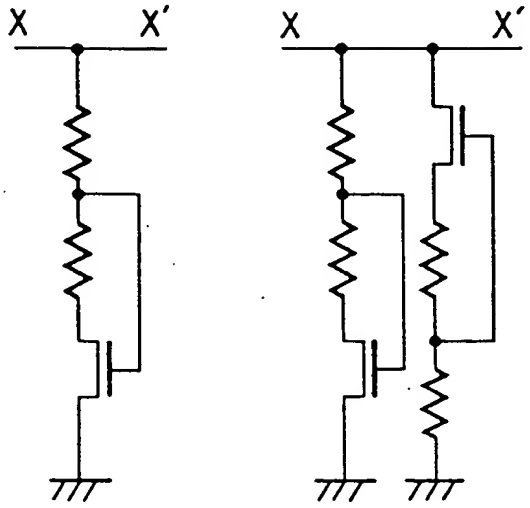


FIG.12(C)

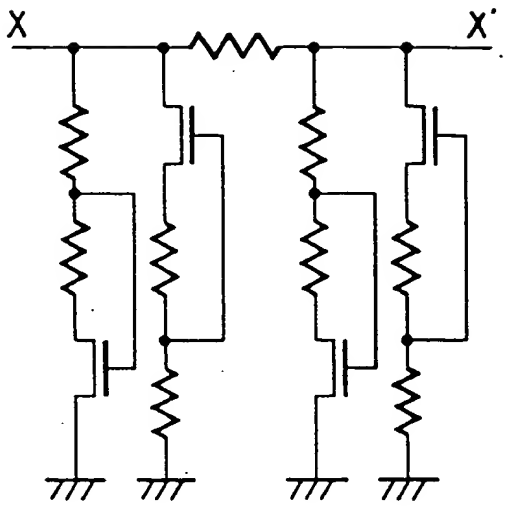


FIG.12(D)

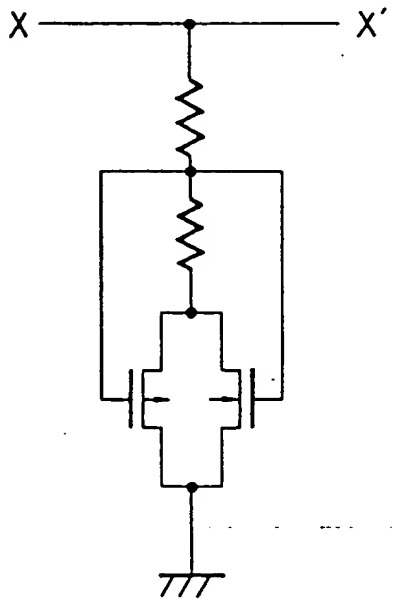
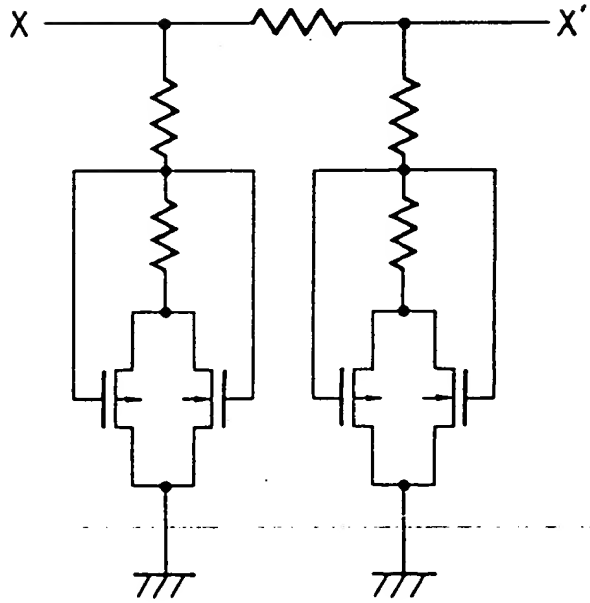


FIG.12(E)



DOCID: 95804560

FIG.13(A)

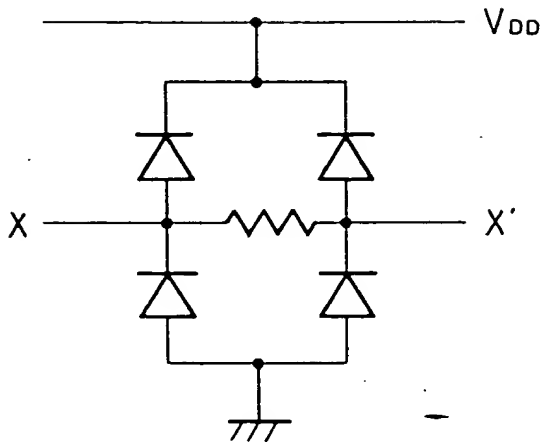


FIG.13(B)

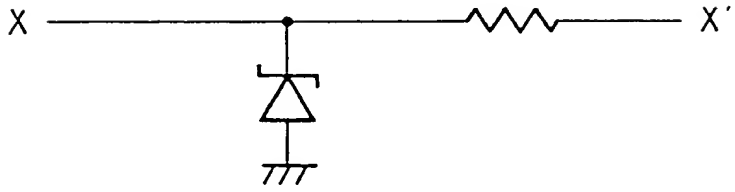


FIG.14

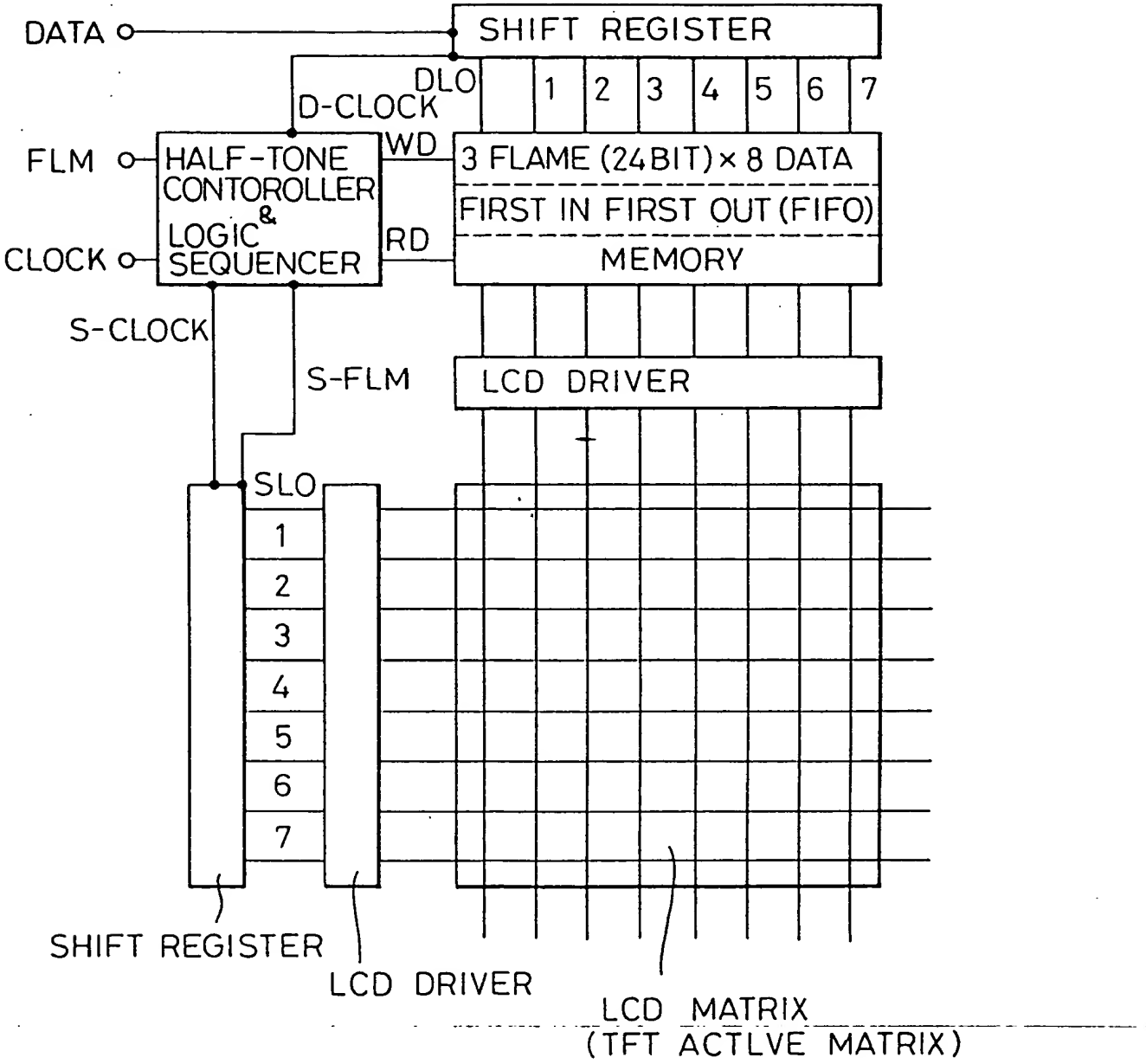

DATA
SHIFT REGISTER
DLO
1
2
3
4
5
6
7
D-CLOCK
FLM
HALF-TONE CONTOROLLER & LOGIC SEQUENCER
WD
RD
3 FLAME (24BIT) × 8 DATA
FIRST IN FIRST OUT (FIFO) MEMORY
CLOCK
S-CLOCK
S-FLM
LCD DRIVER
SLO
1
2
3
4
5
6
7
SHIFT REGISTER
LCD DRIVER
LCD MATRIX
(TFT ACTLVE MATRIX)

FIG. 15

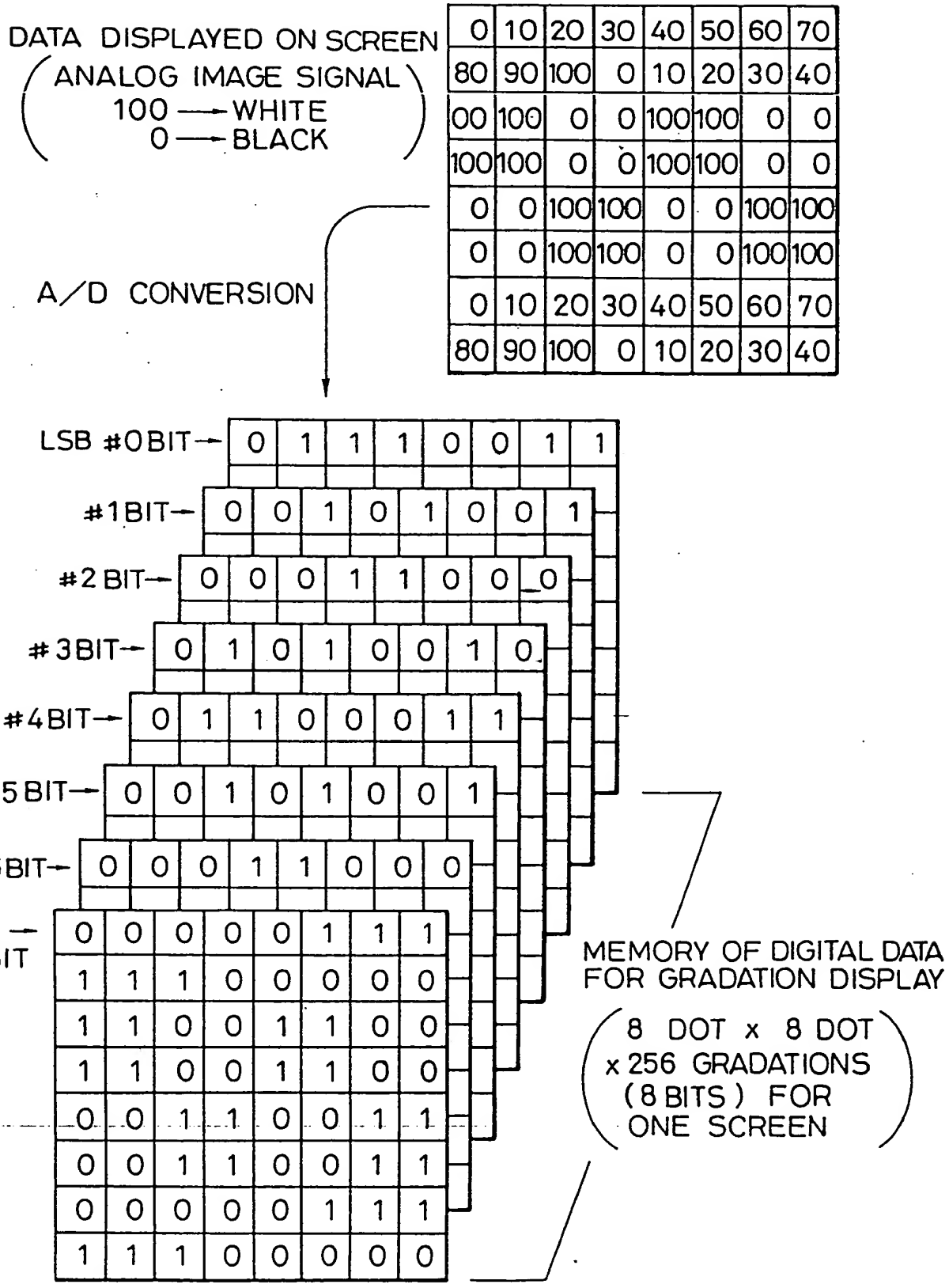

DATA DISPLAYED ON SCREEN
(ANALOG IMAGE SIGNAL
100 → WHITE
0 → BLACK)
0 10 20 30 40 50 60 70
80 90 100 0 10 20 30 40
00 100 0 0 100 100 0 0
100 100 0 0 100 100 0 0
0 0 100 100 0 0 100 100
0 0 100 100 0 0 100 100
0 10 20 30 40 50 60 70
80 90 100 0 10 20 30 40
A/D CONVERSION
LSB #0 BIT → 0 1 1 1 0 0 1 1
#1 BIT → 0 0 1 0 1 0 0 1
#2 BIT → 0 0 0 1 1 0 0 0
#3 BIT → 0 1 0 1 0 0 1 0
#4 BIT → 0 1 1 0 0 0 1 1
#5 BIT → 0 0 1 0 1 0 0 1
#6 BIT → 0 0 0 1 1 0 0 0
#7 BIT → 0 0 0 0 0 1 1 1
1 1 1 0 0 0 0 0
1 1 0 0 1 1 0 0
1 1 0 0 1 1 0 0
0 0 1 1 0 0 1 1
0 0 1 1 0 0 1 1
0 0 0 0 0 1 1 1
1 1 1 0 0 0 0 0
MEMORY OF DIGITAL DATA FOR GRADATION DISPLAY
(8 DOT x 8 DOT x 256 GRADATIONS (8 BITS) FOR ONE SCREEN)

FIG. 16

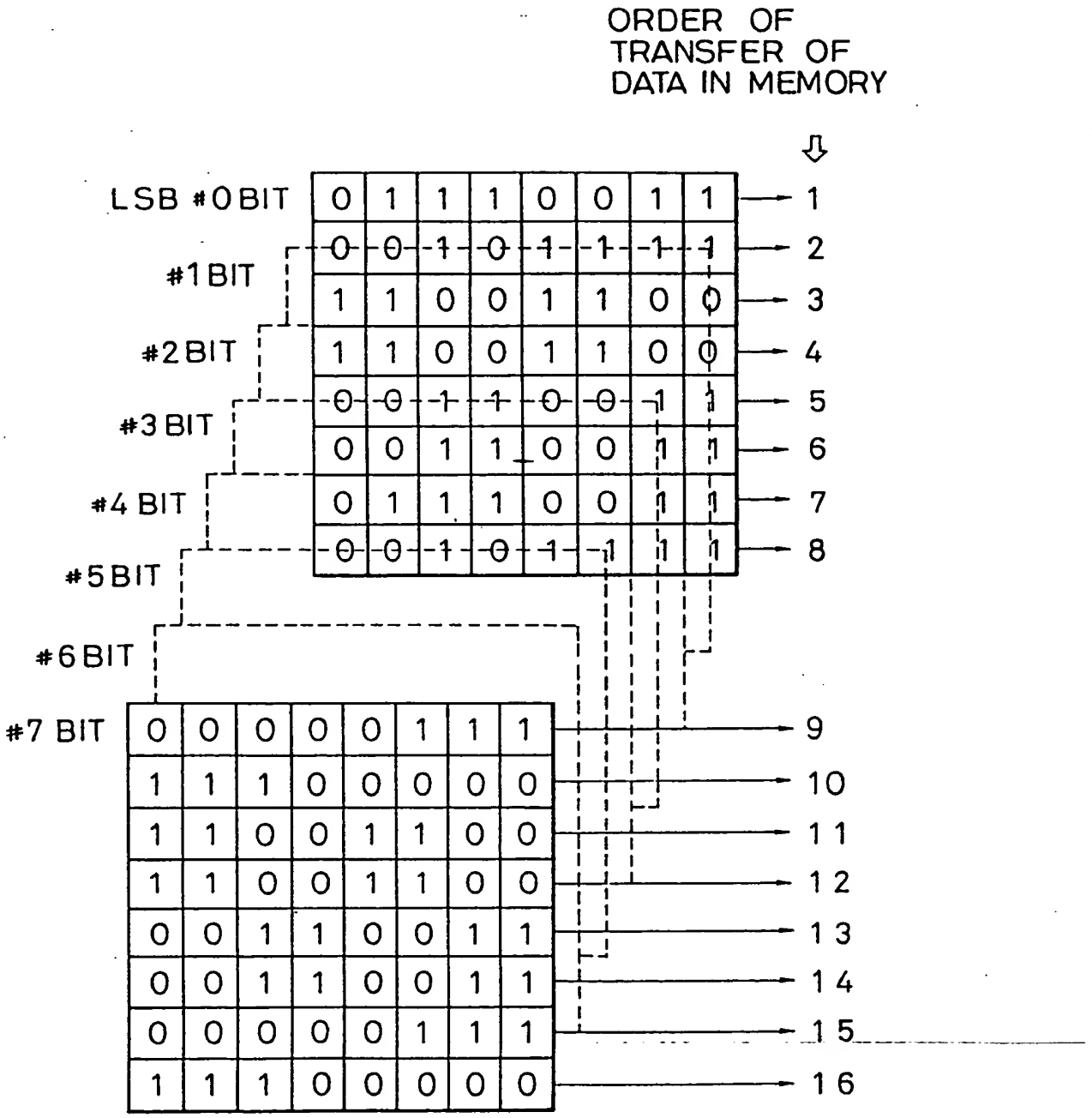

ORDER OF TRANSFER OF DATA IN MEMORY
LSB #0 BIT
#1 BIT
#2 BIT
#3 BIT
#4 BIT
#5 BIT
#6 BIT
#7 BIT
0 1 1 1 0 0 1 1 → 1
0 0 1 0 1 1 1 1 → 2
1 1 0 0 1 1 0 0 → 3
1 1 0 0 1 1 0 0 → 4
0 0 1 1 0 0 1 1 → 5
0 0 1 1 0 0 1 1 → 6
0 1 1 1 0 0 1 1 → 7
0 0 1 0 1 1 1 1 → 8
0 0 0 0 0 1 1 1 → 9
1 1 1 0 0 0 0 0 → 10
1 1 0 0 1 1 0 0 → 11
1 1 0 0 1 1 0 0 → 12
0 0 1 1 0 0 1 1 → 13
0 0 1 1 0 0 1 1 → 14
0 0 0 0 0 1 1 1 → 15
1 1 1 0 0 0 0 0 → 16

FIG. 17

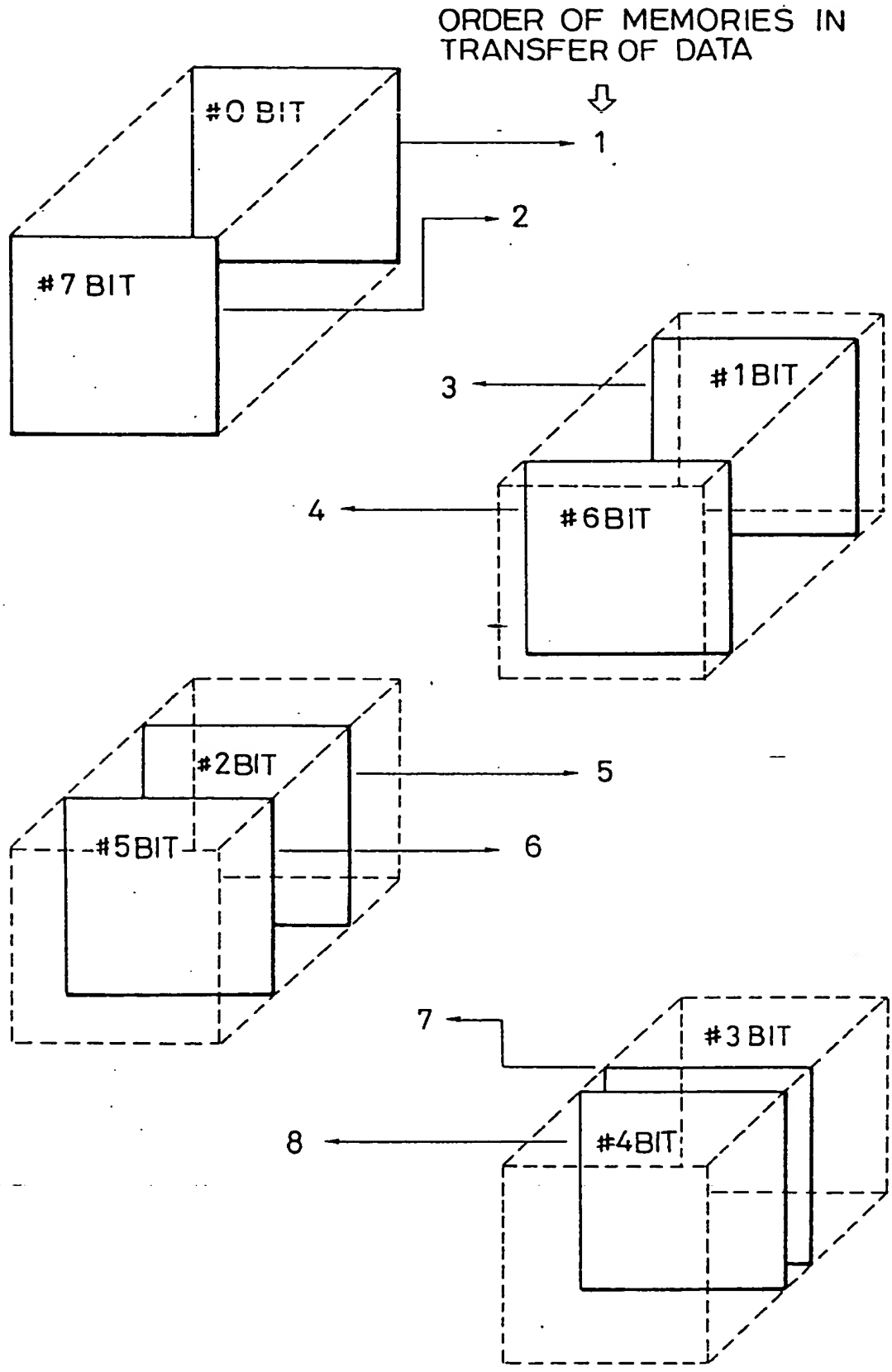
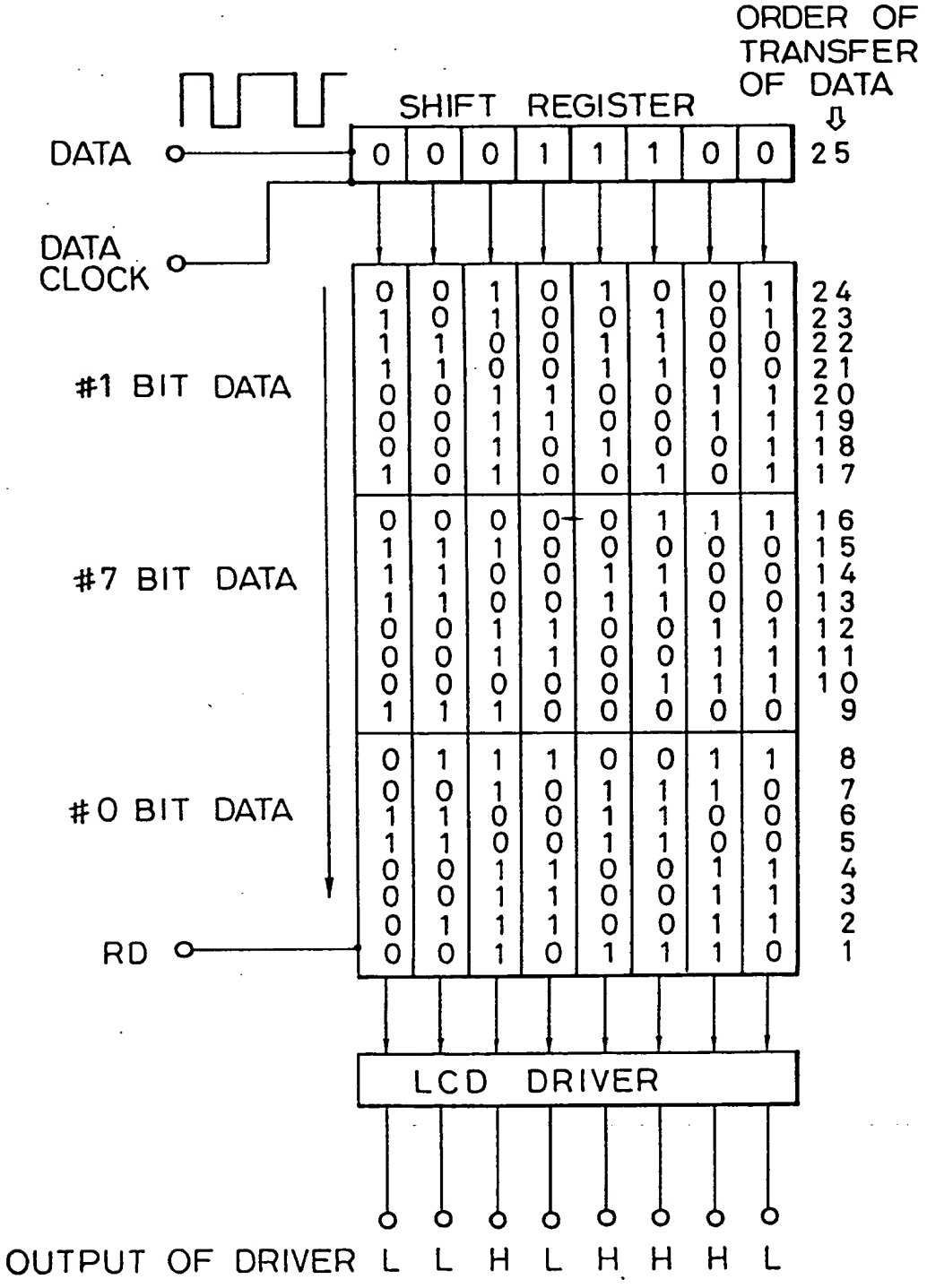

ORDER OF MEMORIES IN TRANSFER OF DATA
#0 BIT
#7 BIT
#1 BIT
#6 BIT
#2 BIT
#5 BIT
#3 BIT
#4 BIT
1
2
3
4
5
6
7
8

FIG. 18


ORDER OF TRANSFER OF DATA
SHIFT REGISTER
DATA
DATA CLOCK
#1 BIT DATA
#7 BIT DATA
#0 BIT DATA
RD
LCD DRIVER
OUTPUT OF DRIVER L L H L H H H L

DOTEC 9680h560

FIG. 19

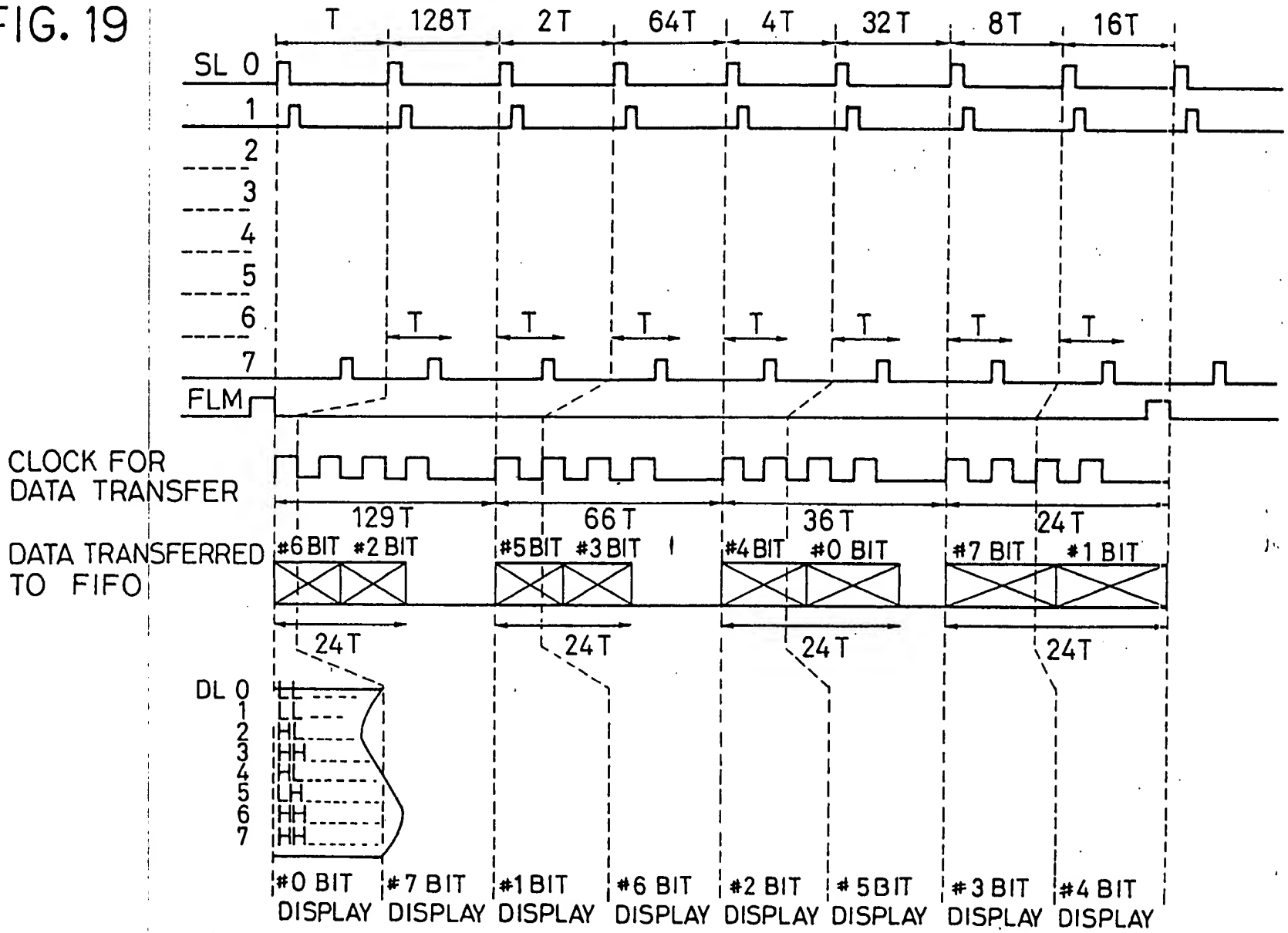


FIG. 20

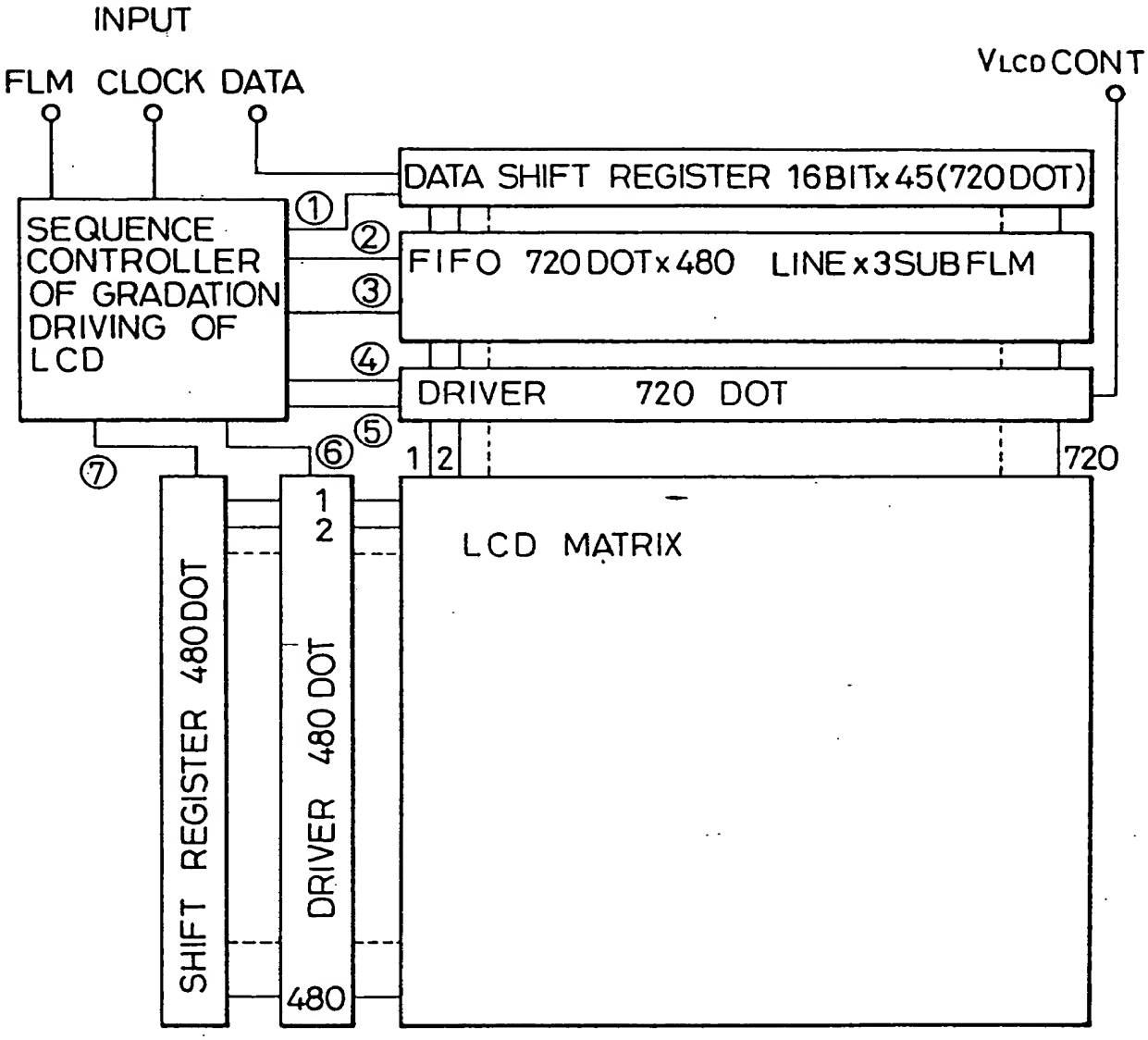

INPUT
FLM CLOCK DATA
VLCD CONT
DATA SHIFT REGISTER 16BITx45(720DOT)
SEQUENCE CONTROLLER OF GRADATION DRIVING OF LCD
FIFO 720DOTx480 LINEx3SUBFLM
DRIVER 720 DOT
1 2
720
LCD MATRIX
SHIFT REGISTER 480DOT
DRIVER 480 DOT
480
① DATA CLOCK
② IN CLOCK
③ OUT CLOCK
④ DRIVE CLOCK
⑤ AC CLOCK
⑥ SET CLOCK
⑦ SHIFT CLOCK

FIG. 21

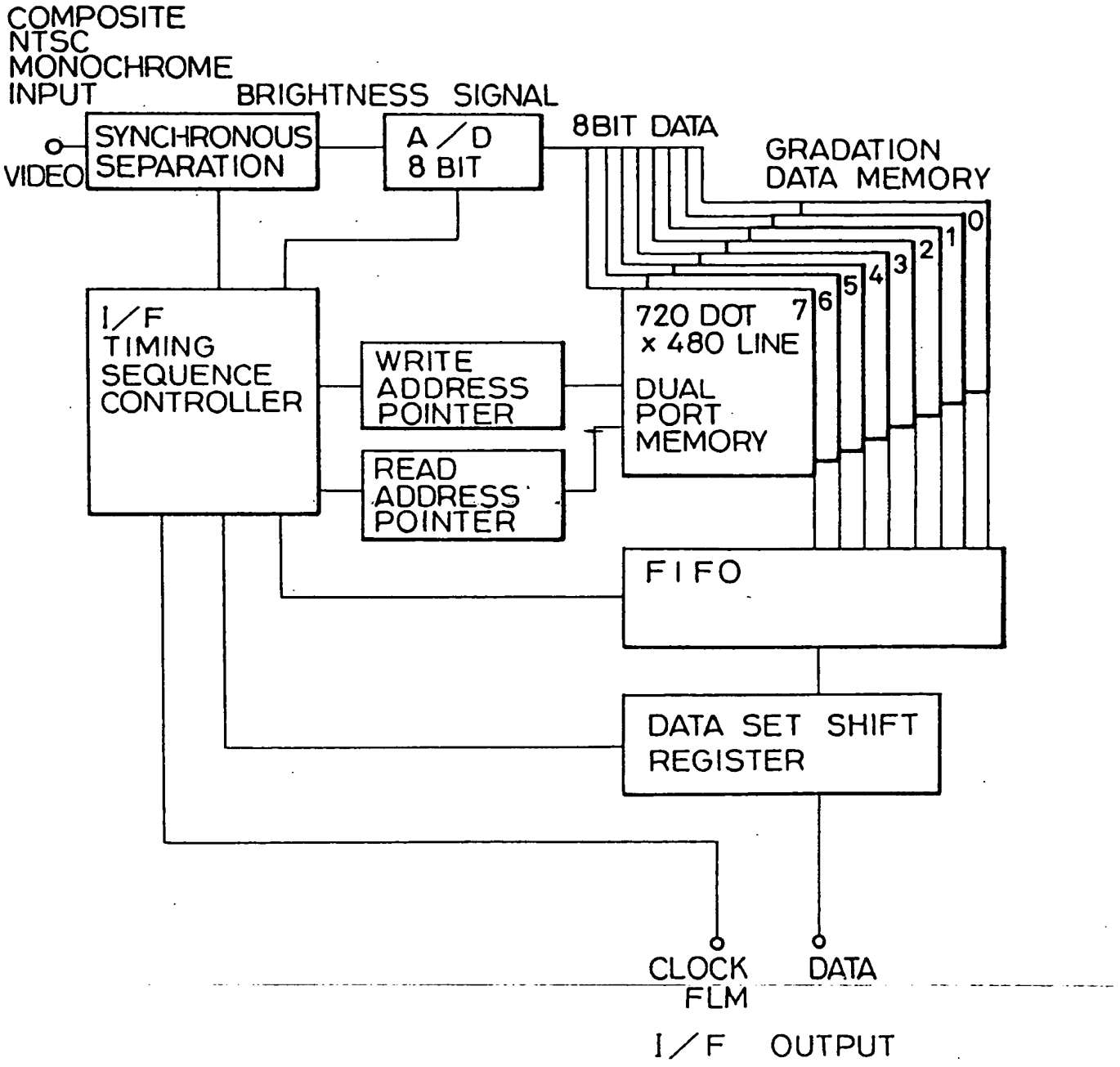

COMPOSITE
NTSC
MONOCHROME
INPUT
VIDEO
SYNCHRONOUS SEPARATION
BRIGHTNESS SIGNAL
A/D
8 BIT
8BIT DATA
GRADATION
DATA MEMORY
0
1
2
3
4
5
6
7
I/F
TIMING
SEQUENCE
CONTROLLER
WRITE
ADDRESS
POINTER
READ
ADDRESS
POINTER
720 DOT
x 480 LINE
DUAL
PORT
MEMORY
FIFO
DATA SET SHIFT
REGISTER
CLOCK
DATA
FLM
I/F OUTPUT

FIG. 22

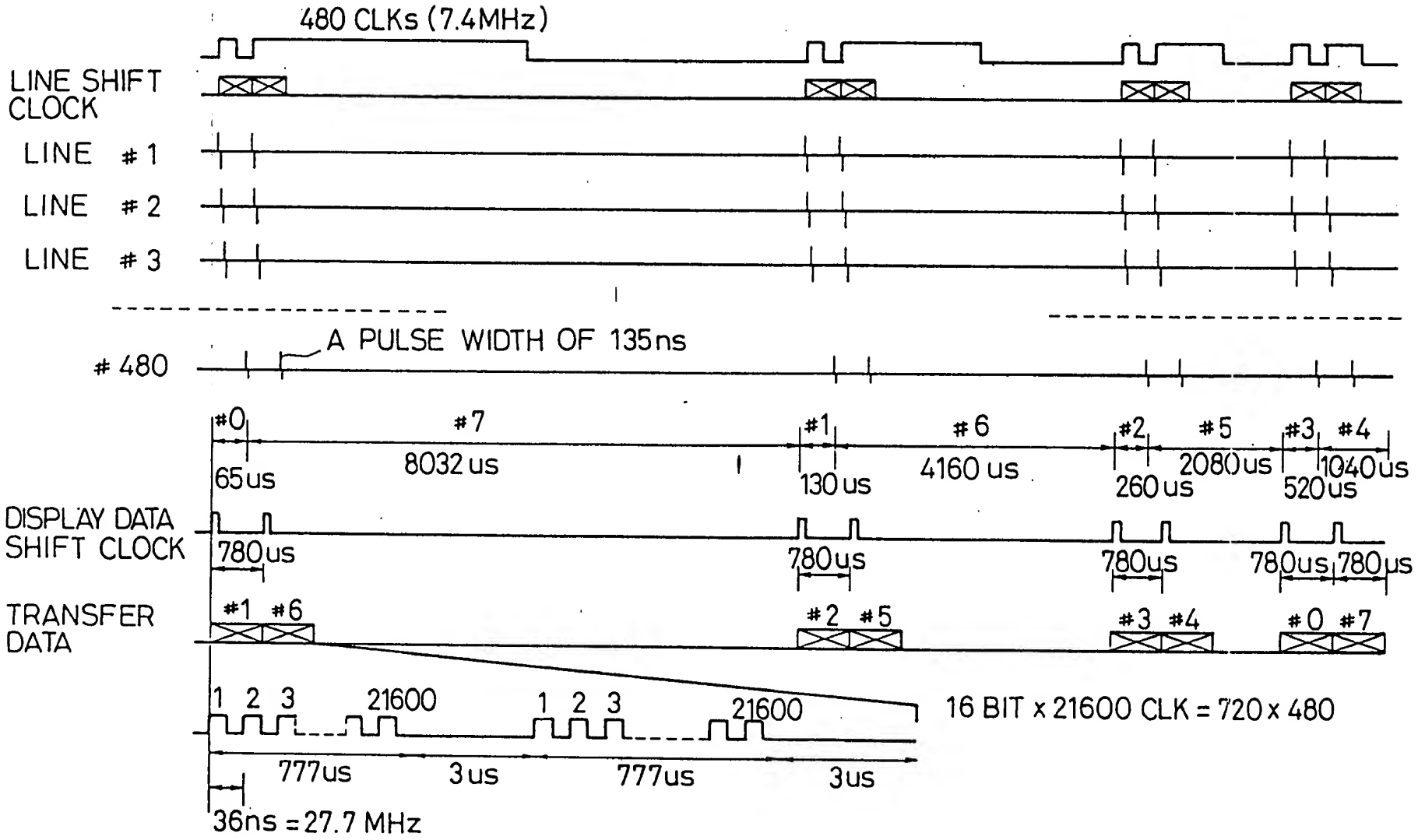

480 CLKs (7.4MHz)
LINE SHIFT CLOCK
LINE #1
LINE #2
LINE #3
#480
A PULSE WIDTH OF 135ns
#0
#7
#1
#6
#2
#5
#3
#4
65us
8032us
130us
4160us
260us
2080us
520us
1040us
DISPLAY DATA SHIFT CLOCK
780us
780us
780us
780us
780us
TRANSFER DATA
#1 #6
#2 #5
#3 #4
#0 #7
1 2 3
21600
1 2 3
21600
16 BIT x 21600 CLK = 720 x 480
777us
3us
777us
3us
36ns = 27.7 MHz

FIG. 23

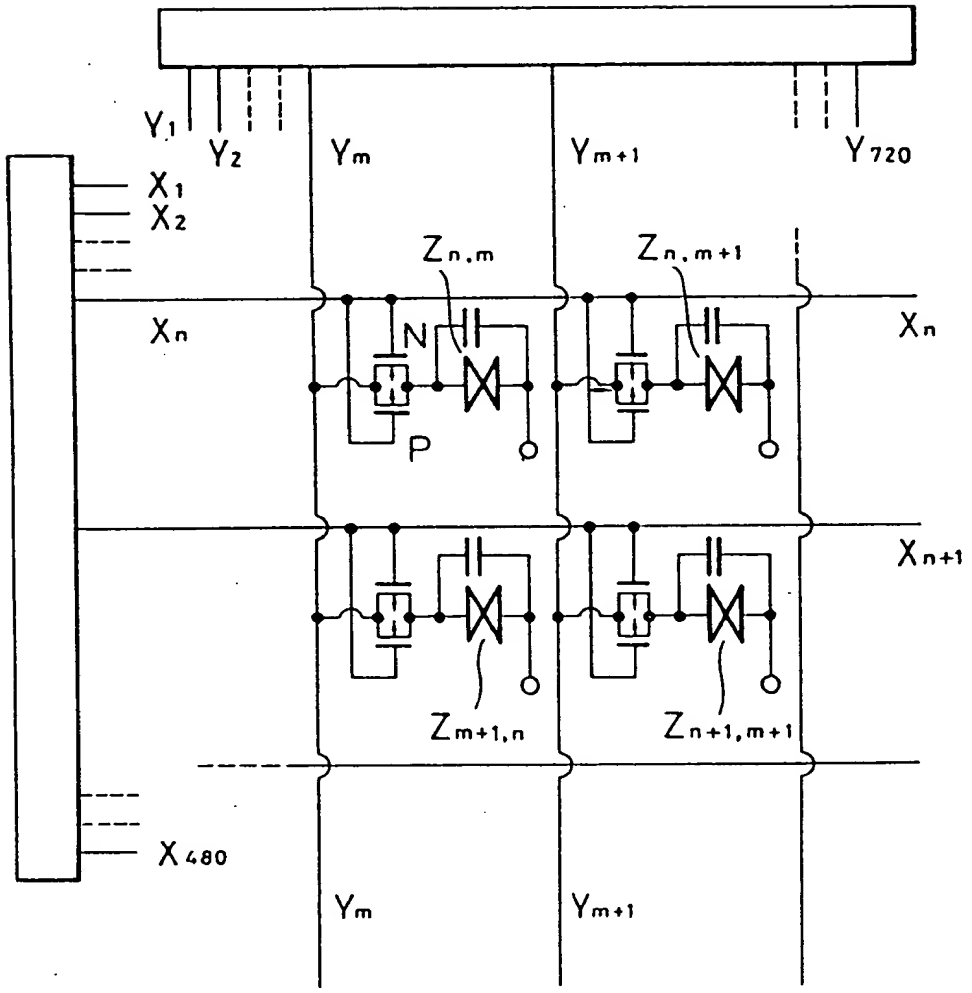

Y1
Y2
Ym
Ym+1
Y720
X1
X2
Xn
Zn,m
Zn,m+1
N
P
Xn
Xn+1
Zm+1,n
Zn+1,m+1
X480
Ym
Ym+1

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FIG. 24

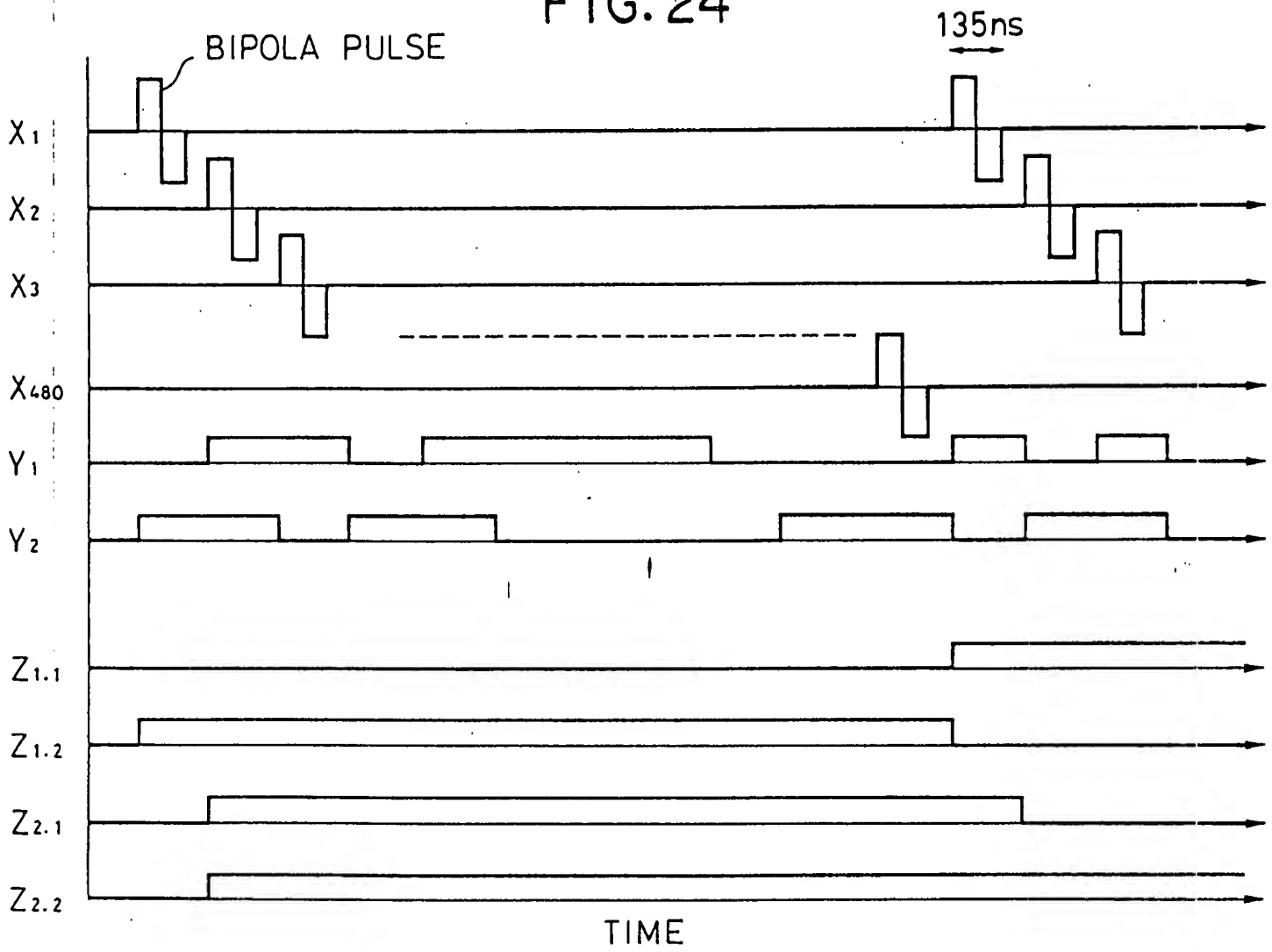
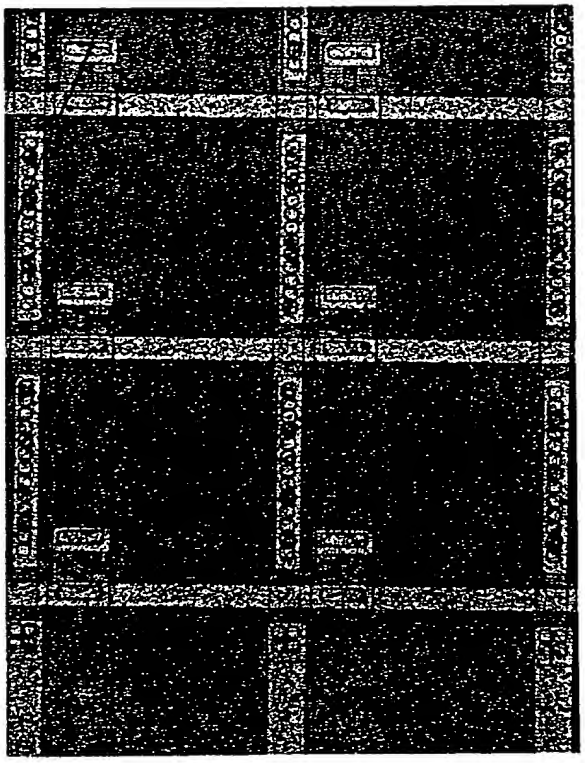


FIG. 25



D956040 - 05-06-95